IN THE SPECIFICATION:

Please replace the paragraph starting on page 2, line 21 of the Specification with the following replacement paragraph:

—An indeterminate clock may exhibit at the receiver system one or more extra clock edges or no edge at all. As discussed above, since[, ,] the clock edge latches the data bits into the receiver latch, the clock edges are usually of most concern. Poor or intermittent connections may cause multiple clock transitions or "edges" – so unwanted clock "signals" occur. If an intermittent mechanical connection exhibits a higher impedance a clock signal may not reach an amplitude sufficient to latch data – so a full clock signal is lost. In such circumstances such clock "errors" are insidious and destructive. Fig. 3 illustrates these issues. A clock signal 30 is shown against an amplitude 32 that represents the amplitude needed to trigger a latch. The leading edge of the clock signal has a characteristic 34 that rises above, below and then again above the threshold 32. If this is the edge that latches data, there may be two latching clock signals where there should only be one. Similarly at the trailing edge of the clock signal 30 ~~thereis~~ there is ringing 36. If this edge latches data there may be two (or more) latching clock signals where there should only be one. Moreover, if there is an impedance or other such anomaly where the amplitude of the clock is reduced 38, the clock signal may not reach the threshold 32 and no clock edge will latch data where there should be one.—

Please replace the paragraph starting on page 3, line 8 of the Specification with the following replacement paragraph:

—It is well known to send along parity or error detection and correction codes, e.g. ECC, that will preserve data bit validity. In one example, parity is a single bit that together with the data bits or a byte or word make the total of the "ones" either an odd or an even number. [.] With simple parity there is no possibility of detecting cases where more than 1 data bit is in error. Additionally, there is no possibility of correcting data bit(s) in error. Well known error correction codes, on the other hand, use additional parity bits that more surely detect errors, and provide the means to correct the majority of the typical errors.—

Please replace the paragraph starting on page 4, line 18 of the Specification with the following replacement paragraph:

—The above disadvantages of the known prior art are addressed by a system where additional or lost clock signals or edges are detected and where the error is generated and presented to the message receiver in near real time without the need to buffer entire messages.—

Please replace the paragraph starting on page 6, line 10 of the Specification with the following replacement paragraph:

—A phase locked loop, PLL, circuit is a feed back circuit that compares and corrects for phase differences between and input signal and a generated feedback signal. The PLL generates a frequency that is compared with the average of an input frequency and "locks into" that frequency by driving the phase error to zero (although there may be a set phase difference between the input and the generated frequencies). The PLL is well known in the art and has the distinction of being applicable for many different purposes. But typical applications can be broadly classed as a) frequency re-creation and multiplication, and narrow-band filtering – based on the ability to respond to an input frequency; and b) frequency modulation/demodulation – based on the ability of the phase detector and the internal voltage controlled oscillator (VCO) found in PLL's to respond to a DC voltage. In the present invention, the PLL is designed for the first (a) above listed use.—